REMARKS/ARGUMENTS

A petition and fee is filed herewith for a one month extension until 01/09/2005.

In DETAILED ACTION, Oath/Declaration the examiner states that the oath or declaration is defective. A telephonic interview with Examiner Payton was conducted on November 8, 2005 in which curing of the defective declaration was discussed. No claims were discussed. The examiner's courtesy in explaining the correction of the defective declaration is hereby acknowledged, with thanks. A corrected declaration is included herein.

In Claim Rejections - 35 USC § 112, claims 2 and 18 are rejected as there is no discussion of the limitations JTAG, USB and I^2C I/O devices. These type devices are clearly shown in Fig. 4, which schematically depicts a software structure with a DAL according to the present invention (see paragraph **[0036]**). Paragraph **[0042]** has been amended to identify these devices. As pointed out by the examiner in the office action, these types of I/O devices are well known. It is therefore submitted that including a reference to the devices in the specification is not new matter as these type devices are clearly shown in Fig. 4 and included in claims 2 and 18, which are part of the disclosure as filed. It is submitted that the specification, as amended, does provide sufficient antecedent basis for the limitation in claims 2 and 18, and that claims 2 and 18 are now allowable under 35 U.S.C. 112, which allowance is respectfully requested.

Under Claim Rejections - 35 USC § 103, claims 1-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morelli et al., (US 6,438,737), hereinafter Morelli.

Morelli discloses a reconfigurable logic circuit having programmable logic responsive to an interface program to provide a number of interface buffers in a memory operable to store data passing between a computer and the reconfigurable logic circuit (see abstract). In Morelli, application programs 112 requests to utilize reconfigurable logic circuit 40 may result in a number of coexisting virtual program interfaces. Each of these virtual program interfaces communicates with reconfigurable logic circuit 40 through a set of standard routine that treat each logic design instance in a manner comparable to a logical file. Logic interface program 122 manages the virtual program interfaces in a file-like manner. A logic interface program 122 communicates these standard command/functions through device driver routine 124. Device driver routine 124 generates each read or write access to which reconfigurable logic circuit 40 responds. Computer interface logic portion 54 of programmable logic 50 monitors porcessor bus 24 for an appropriate read or write access to memory space RL by device driver routine 124. If a valid access is detected, reconfigurable logic circuit 40 responds in accordance with the command, request, or data communicated by computer 22. (See Col. 8, lines 37-56.)

In the present invention, remote device resources are mapped into a microprocessor I/O address space or memory address space as if the remote device was locally available to the microprocessor (paragraph **[0025]**). An exception is generated during instruction execution upon accessing a mapped virtual resource that does not physically exist (paragraph **[0039]**). An exception may be generated in one of two ways; (1) upon accessing a memory location where no real memory is mapped (paragraph **[0037]**), and (2) upon execution of a privileged instruction (paragraph **[0040]**). The Device Abstraction Layer (DAL) facilitates the virtualization of the remotely attached device

and makes it appear to the device driver software as if it was locally attached to the microprocessor bus (paragraph **[0042]**). Access to the relevant address range cause an exception (paragraph **[0045]**) which exception may be handled by the DAL. The Exception Handler transfers control to the DAL and provides sufficient information for the DAL to decode the operation that the device driver actually wanted to perform with the device (paragraph **[0047]**).

Claims 1, 11 and 17 have been amended to claim generating an exception upon accessing a mapped virtual resource unit, and handling the exception with an exception handler to operate the remote I/O devices as if locally attached to the embedded microprocessor. There is no teaching or suggestion in Morelli that an exception be generated upon accessing a virtual resource unit, or that an exception handler handle such exceptions to operated the remote I/O device as if it was locally attached. Claims 7 and 23 have been amended to claim a method and program product wherein the claimed DAL uses the memory management unit to cause a program exception which is handled by the exception handler. Claim 15 is amended to claim a computer system wherein the exception generating unit is software adapted to cause a program exception as soon as resources are accessed. Claims 9 and 25 claim a method and program product claiming generating an exception during instruction execution, and claims 10 and 26 claim a method and program product wherein the instruction is a privileged instruction. It is respectfully submitted that claims 1-26, as amended herein, are allowable under 35 U.S.C. 103 over Morelli, which allowance is respectfully requested.

It is respectfully submitted that the application is now in condition for allowance, which allowance is respectfully requested.

RESPECTFULLY SUBMITTED

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